Silicon pixel detectors for particle physics

Joost Vossebeld

UNIVERSITY OF
LIVERPOOL

Disclaimer

There is a lot of amazing development work on pixel detectors.

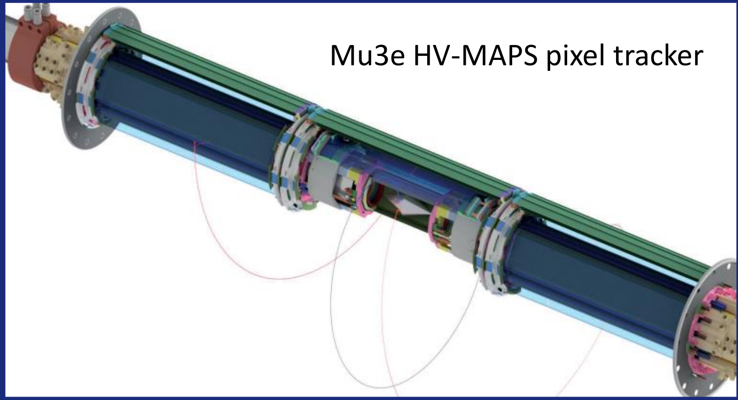
I have worked more on developing, building and operating silicon detectors than on silicon R&D itself.

I've chosen to focus today on the main challenges for future experiments and discuss the main directions of R&D to address these.

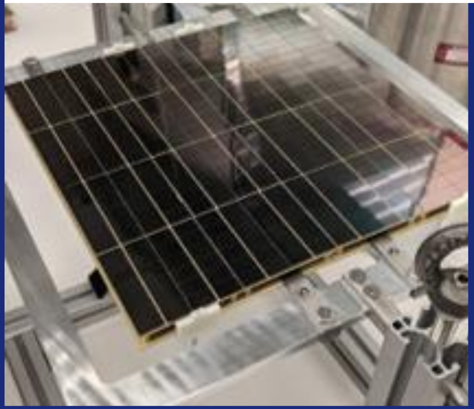
Examples I show are heavily biased by experiments I am involved with or happen to know about.

ATLAS Semi-Conductors Tracker (SCT).

Mu3e HV-MAPS pixel tracker



SiPM Photon Detector Module DarkSide20k



Scope of this seminar

1. Performance challenges for silicon tracking sensors
2. The basic pixel technology options for experiments
    1. Hybrid (planar) pixel sensors
    2. Monolithic CMOS pixel sensors
    3. 3D integration
3. Solution development for specific performance challenges
    1. radiation tolerance
    2. fast timing (4D tracking)
    3. position resolution (novel concept)
    4. Minimising material

Performance challenges for silicon tracking sensors

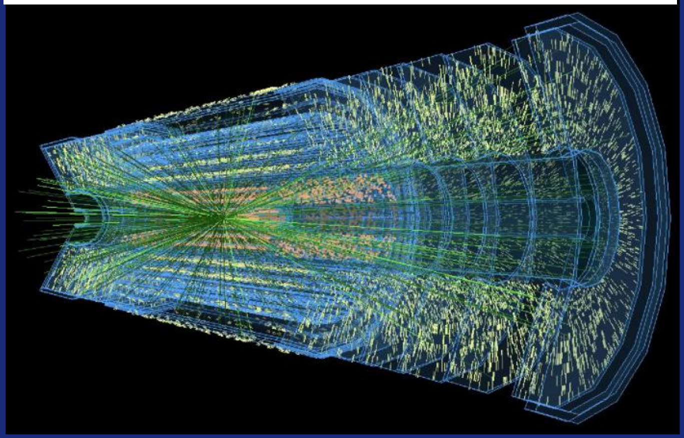
Key performance challenges

Future hadron-hadron colliders

(HL-LHC and FCC-hh, other high rate experiments, beam monitoring, proton therapy instrumentation, ..)

Assumed that after HL-LHC both vertexing and tracking will rely on pixel sensors

simulated event at the HL-LHC (pile-up = 200)



Innermost layers

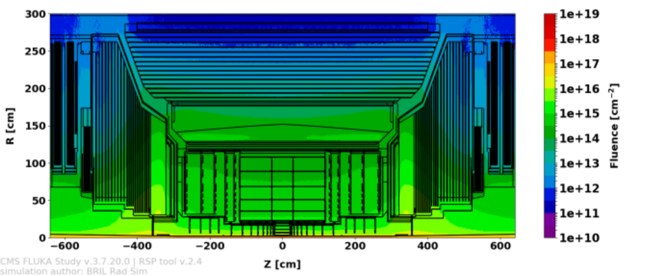
- **Small granularity**: to cope with high occupancy
- **Radiation tolerance**: HL-LHC few times 10^{16} n_{eq}/cm^2 ; FCC-hh ~10^{17} n_{eq}/cm^2
- **Timing resolution**: (for 4D tracking): O(30 ps)
- **Small area**: cost is less critical

Outer layers

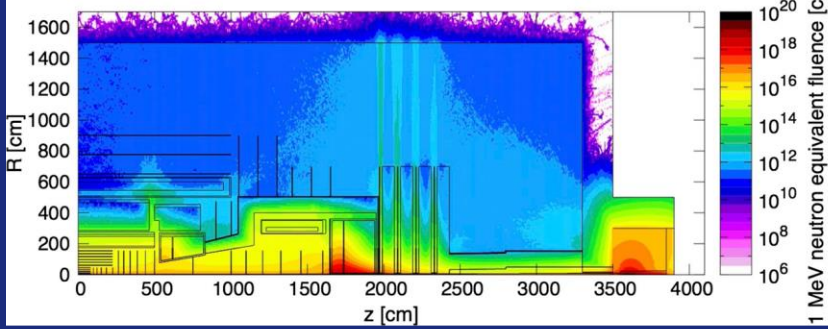
- **Small granularity**: to cope with high occupancy
- **Radiation tolerance**: 10^{15}-10^{16} n_{eq}/cm^2
- **Large area** : requires cost-effective technology for large area coverage O(100 m^2)

HL-LHC is the main testbed for the R&D to meet future requirements!

CMS: Integrated dose during HL-LHC



Integrated dose FCC-hh



Key performance challenges
Future e^+e^-

(ILC, CLIC, CEPC, FCC-ee, but also heavy ions ALICE/EIC, and non-collider precision experiments)

Vertexing

- **Excellent position resolution**: ~2-3 µm resolution for e^+e^-
- **Ultra-low material**: thin devices <0.1%X_0 and also low power to allow air cooling
- **Readout speed**: ~500 ps for CLIC or circular options.

Tracking

- **low material:** thin devices and low power
- **Large area deployment**: cost-effective technology for large area coverage

In addition to HL-LHC, Heavy ion and other precision experiments are a key testbed for the R&D to meet these requirements

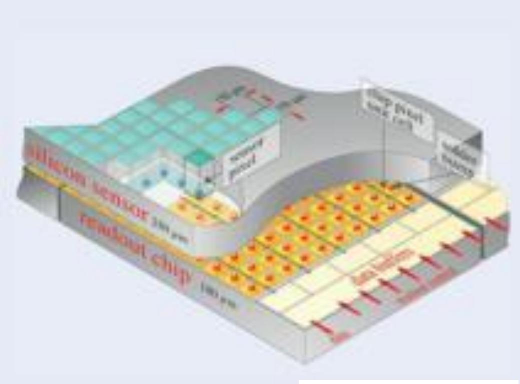
The main pixel concepts

Hybrid pixel sensors

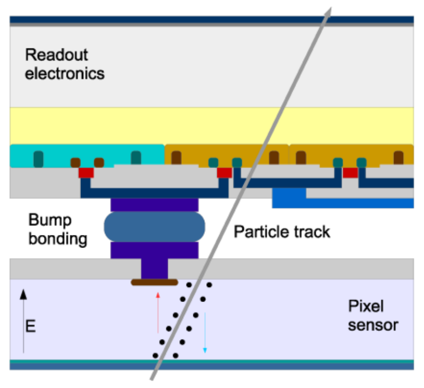
CMOS MAPS

3D stacked sensors

Hybrid pixel detectors



T Rohe, PSI



Instruments **2020**, *4*(4)

The most common hybrid pixel sensor

- Pixelated planar (mostly but not necessarily) silicon sensor
- A readout ASIC with contact pads matching the 2D pixel layout
- Connections are made with fine-pitch chip-to-chip bump-bonding

Important advantages

→ combination of mature technology sensor options with high level functionality front end (RD53, VeLopix, Timepix, ..)

Drawbacks

→ Need for bump-bonding limits the minimal pixel pitch and thickness

→ Cost /complexity challenging for large area deployment

Baseline technology deployed in most challenging (high rate / high radiation) detectors (e.g. LHC vertex layers)

Implementation of hybrid pixel detectors

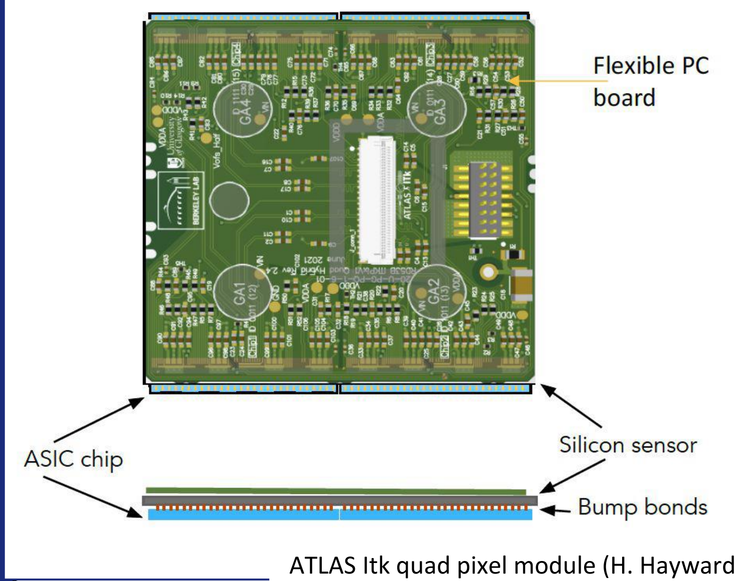
An example of a typical detector

<ins>**ATLAS ITK pixel layers**</ins> (Quad modules)

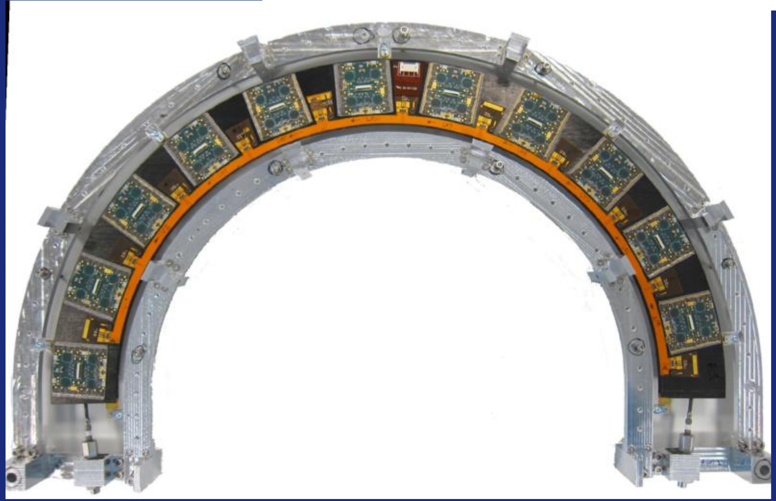
- Module
  - 4 x 4 cm^2 planar sensors with 50x50 µm^2 pixels, 100 to 150 µm thick
  - Bump-bonded to four RD53 readout ASICs, 150 µm thick
  - Mounted to a flexible PCB

- Multiple module mounted on mechanical supports hosting electrical services and cooling

Even with thinned sensors the final overall detector stack has substantial material



ATLAS Itk quad pixel module (H. Hayward, vertex 2022)



Monolithic CMOS sensors

Single devices

→ ease of assembly and testing

→ Low material (sensors thickness down to 50 µm)

→ low power (in standard CMOS processes)

Industry standard process(es)

→ less scope for sensor optimization compared to hybrid sensors

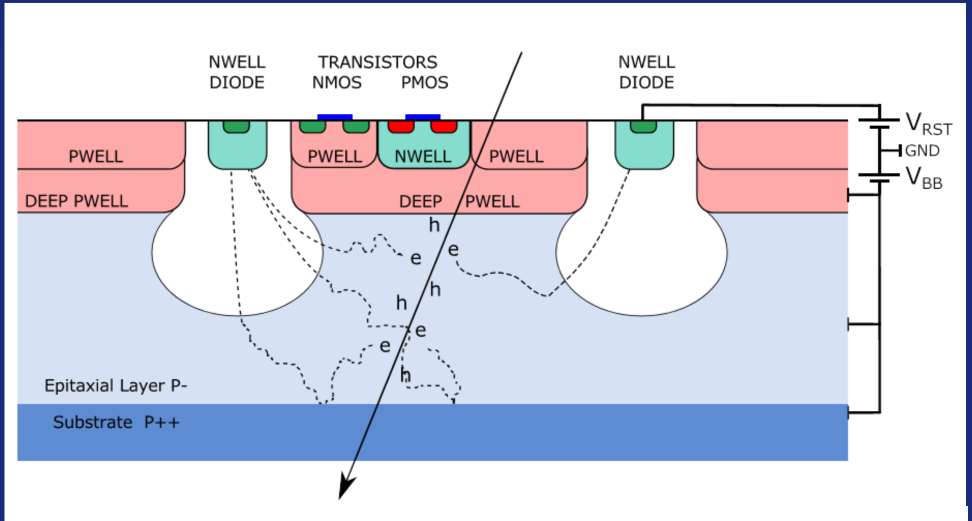
→ “cost effective” (low production cost, but high development cost)

→ high throughput at foundry

Main limitations (charge collection by diffusion from non-depleted areas)

→ limited speed

→ Limited radiation tolerance



ALICE Collaboration, Journal of Physics G 41 (2014) 087002.

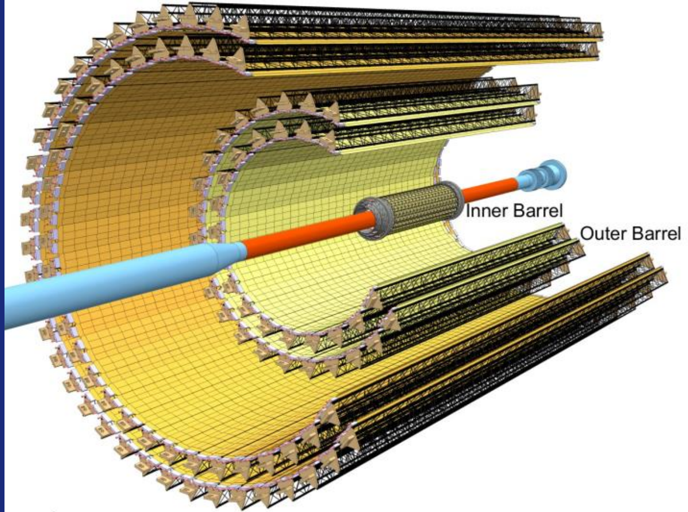
Go-to solution for high performance vertexing/tracking when radiation tolerance constraints are more relaxed.

Implementation of CMOS MAPS

The ALICE heavy Ion experiment operates at moderate (~500 kHz) interaction rate, but high particle density events.

Key requirements are

- Low material
- Excellent position resolution



ALICE Collaboration

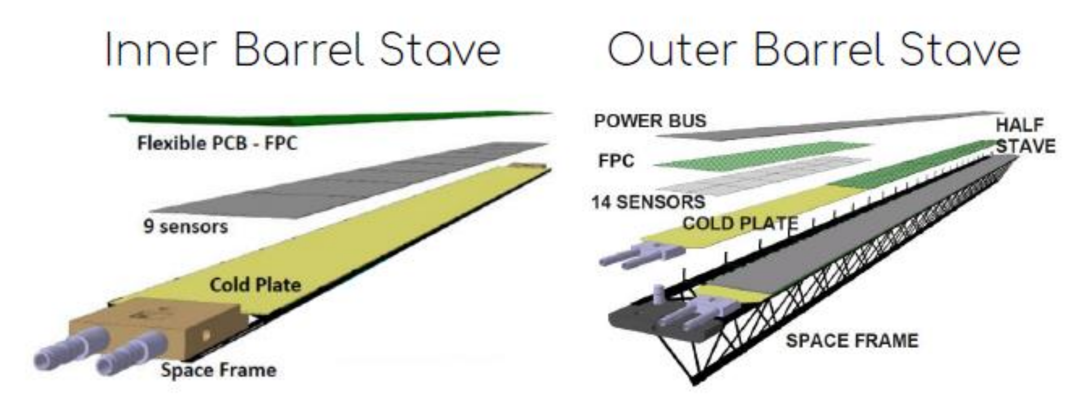
Ivan Ravasenga, VERTEX 2022

ALICE ITS2 MAPS pixel tracker

Based on the ALPIDE MAPS sensor (~1.5x3 cm^2)

- Module with 9 or 14 sensors are mounted on low mass supports with integrated cold-plate
- Very low material budget achieved:
  - 0.36% X_0 inner barrel (50 µm sensors)
  - 1.14% X_0 outer barrel (100 µm sensors)

Substantially lower material achievable compared to hybrid sensors



3D stacked pixel sensors

Combines some of the advantages of hybrid pixel sensors and CMOS MAPS

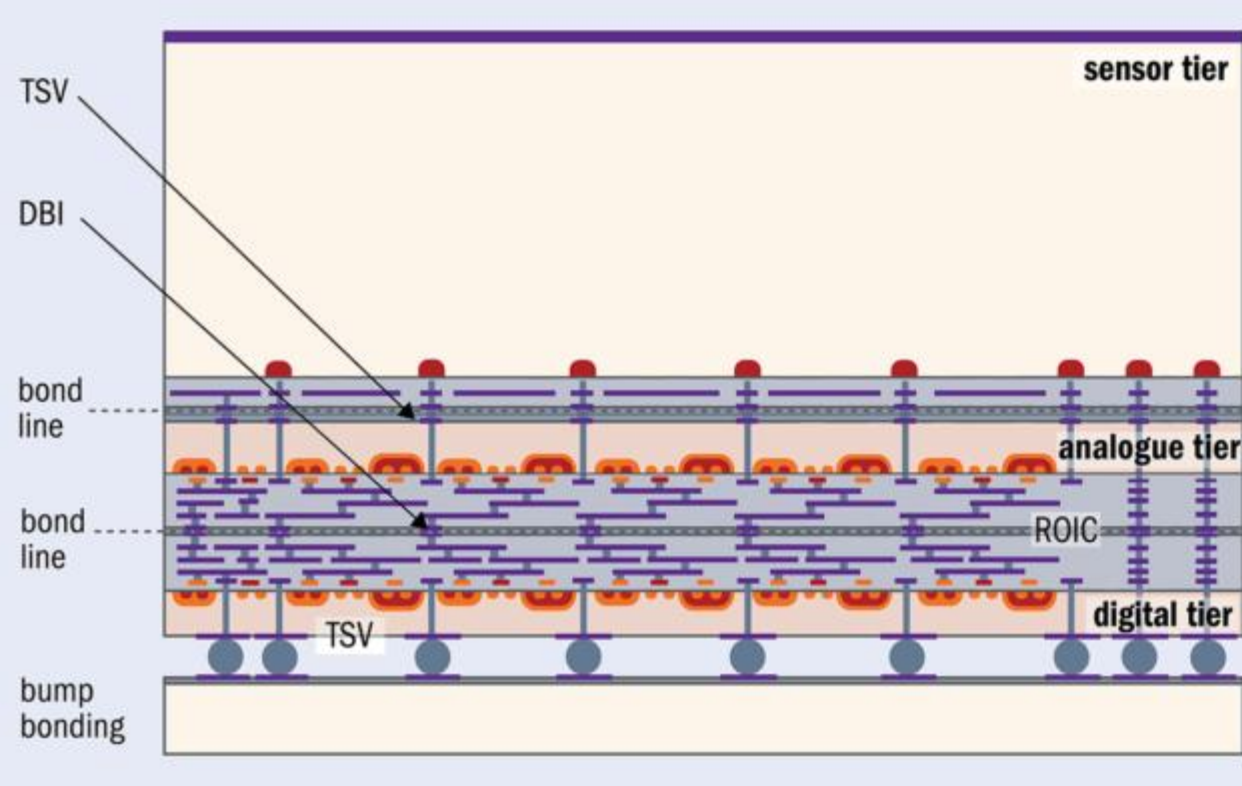
- Vertical stacking allows for high level of complexity without analogue and digital electronics competing for space
- No need for bump-bonding removes constraints on pixel size and device thickness
- Different technology for sensor and electronics layer
- Short (vertical) path lengths

Main limitation:

- Complex less easily accessible technology (costly)

Technology option for most challenging (small area) detector

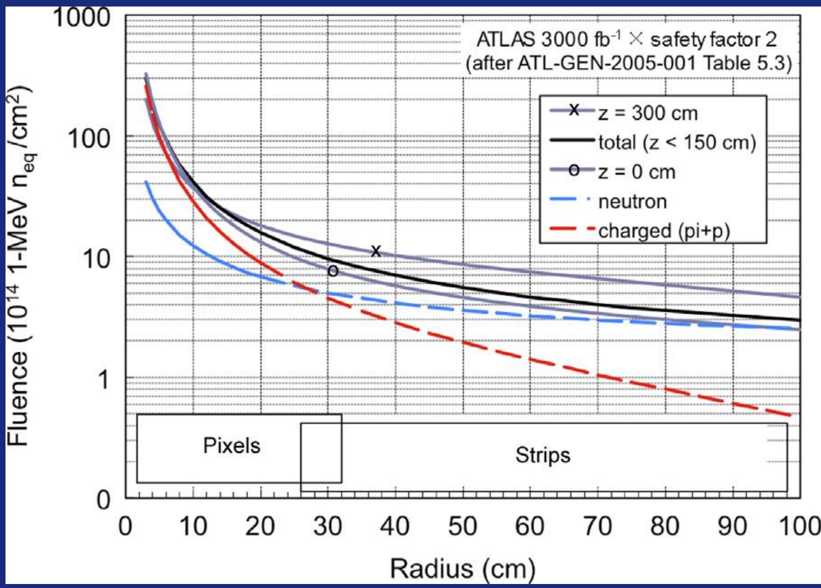
CERN Courier, Jul 2021



Radiation tolerance

Radiation tolerance

HL–LHC will see radiation levels up to few times 10^{16} 1 MeV neq/cm^2
(..and up to 10^{17} neq/cm^2 at a future FCC-hh facility)



Large programme of R&D carried out for LHC and HL-LHC led to improved understanding and modelling of damage mechanisms and effects.

Key effects of radiation damage include:

- Changes to effective doping concentration
- Introduction of level in the band gap that cause trapping / leakage current

These lead to:

- Changed doping concentrations and reduced depletion depth
- Increase leakage currents (more noise, risk of thermal runaway)
- Reduction and delay of the collected signal

Many mitigation strategies were developed

Radiation tolerance in hybrid planar pixel sensors

R&D has delivered a “baseline” solution for the planar hybrid pixel sensors used across the HL-LHC upgrades of ATLAS, CMS, LHCb.

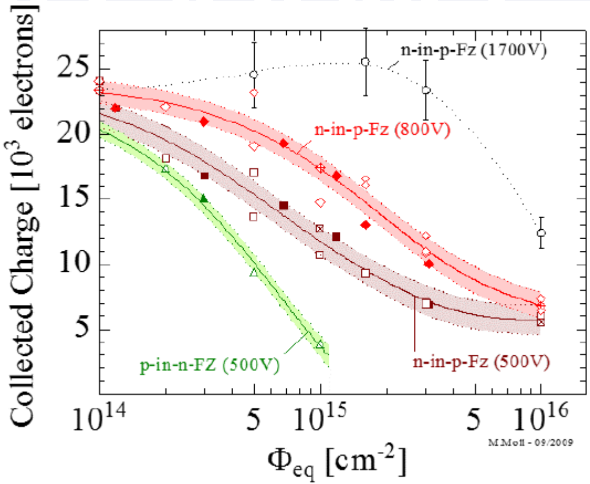
1) pixel sensors with n-in-p diode structure on high resistivity wafers → *electron readout & depletion from the readout side.*
2) Sensor design optimised for high bias voltages (up to ~1000V) → to *recover lost depletion depth*
3) Frontend electronics implemented in small technology nodes for high level functionality (e.g. RD53, VeLoPix)
4) R&D on bump bonding ensured high yield bonding at small pixel

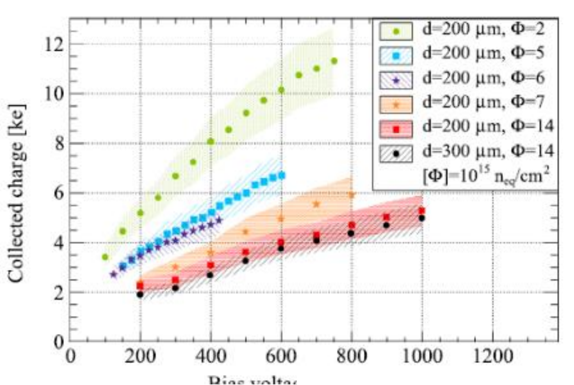
Radiation tolerance planar pixel sensors demonstrated to high Fluences

<u>ATLAS ITk pixel modules</u>

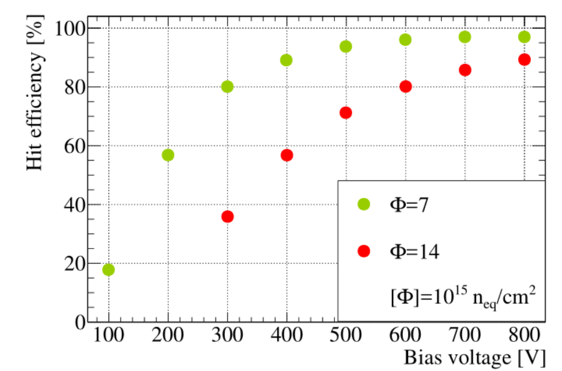
- > 99% hit efficiency at 600 V after 5x10^{15} n_{eq}/cm^2
- At around 10^{16} n_{eq}/cm^2 efficiency drops below 90%

Sufficient for all but the innermost layers





NIM A 831 (2016) 111–115



N. Wermes HSTD 11, Hiroshima

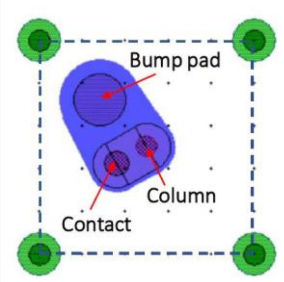
UNIVERSITY OF LIVERPOOL

3D pixel sensors

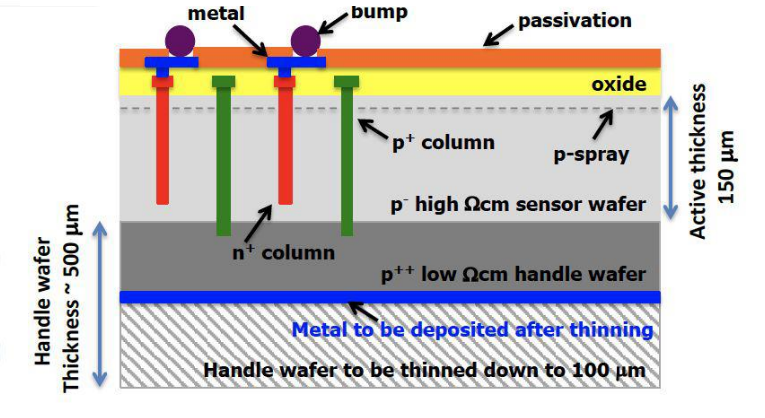
The innermost pixel layers at the HL-LHC sensors are exposed to dose rates beyond 10^{16} n_{eq}/cm^2 (similar or more for future LHCb vertex locator, FCC-hh).

3D sensors deploy n and p type doped pillars in p bulk

- Deletion zone between pillars with horizontal E-field direction.
- Collection distance is shortened (without loss of signal!)



G.F. Dalla Betta et al., NIMA 824 (2016) 386



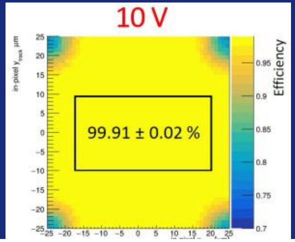
Can be implemented as hybrid pixel sensors

- Demonstrated radiation tolerance beyond 10^{16} n_{eq}/cm^2

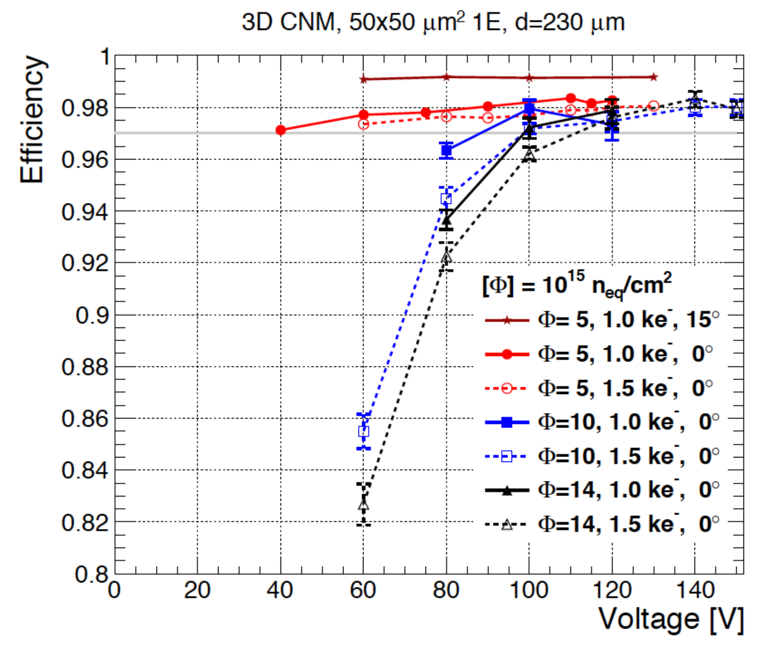
Main drawbacks are

- Some efficiency losses around the p-type pillars (reduced with sensors tilt)
- Added complexity of sensor manufacture

Deployed e.g. in ATLAS IBL and innermost layers ITK



Lapertosa IWoRiD 2022



arXiv:1707.01045

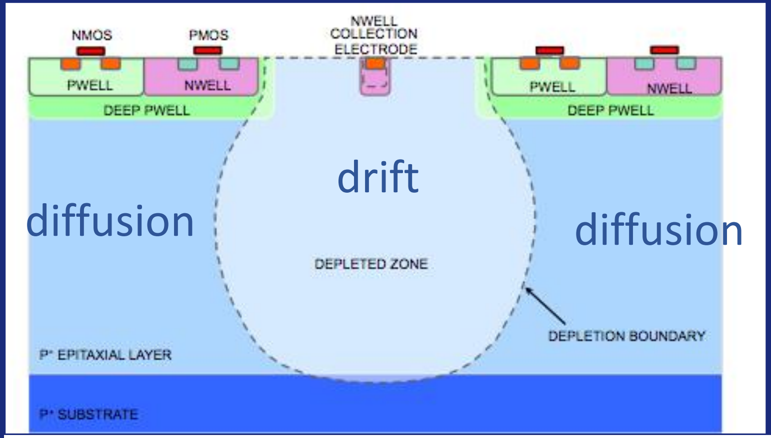
Radiation tolerance in CMOS monolithic pixel sensors

Depleted Monolithic Pixel Detectors (DMAPS)

MAPS sensors have obvious advantages over hybrid sensors in terms of material budget, cost, speed-of-production, ease-of-manufacture.

But standard CMOS MAPS do not survive at high radiation doses (e.g. ALPIDE ~10^{14} n_{eq}/cm^2).

The main reason is the lack of a fully depleted region from which charge is collected.

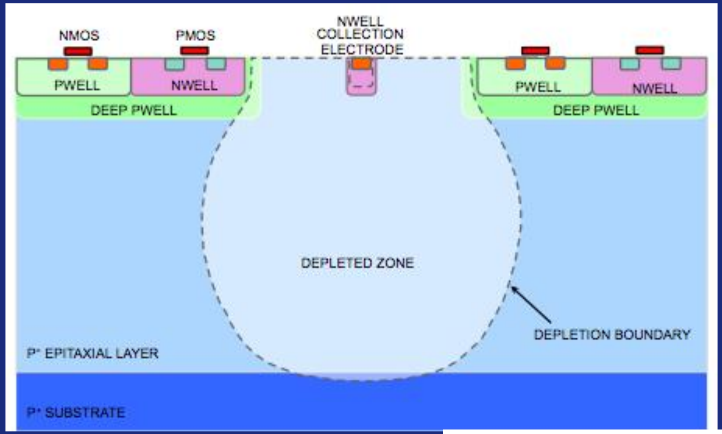


ALICE Collaboration, Journal of Physics G 41 (2014) 087002.

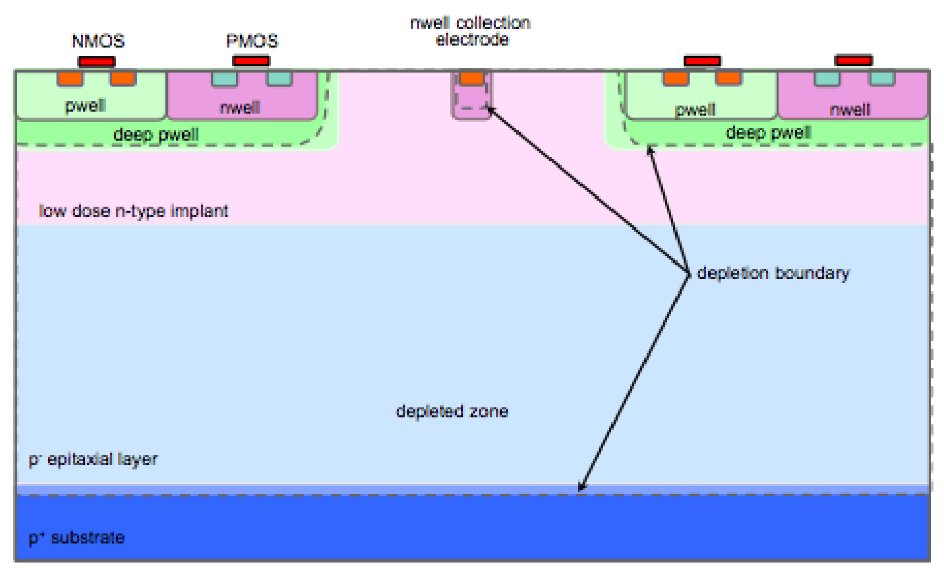
Achieving full depletion in CMOS promises faster and more radiation tolerant MAPS.

There are two key approaches..

Small diode / moderate voltage depleted CMOS



Sensors **2008**, *8*(9), 5336-5351;



NIM A 871 (2017) 90–96

MALTA chip: developed from ALPIDE chip using a modified TowerJazz 180nm CIS process

(the same process was also used for TJ-Monopix / CLICPIX)

Added low dose n-implant ensure a fully depleted epitaxial layer → charge collection by drift (horizontal!)

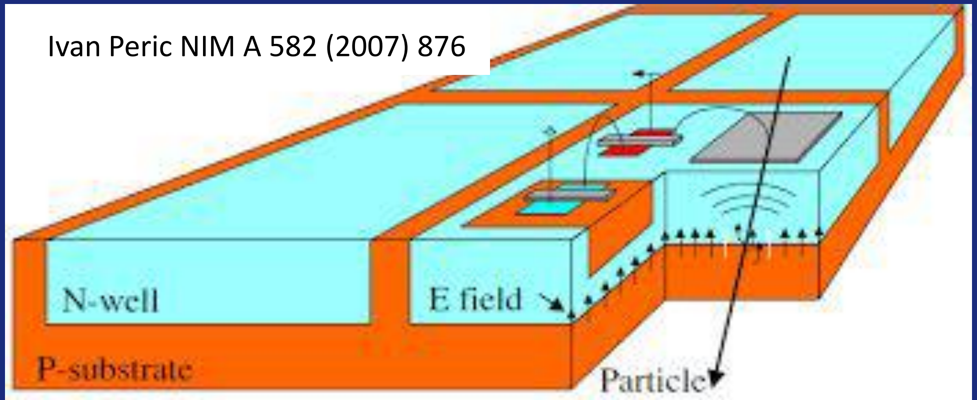
- Small collection diode (low noise, low power)
- Charge collection time ~1ns
- Operation up to 1×10^{15} n_{eq}/cm^2
- Some inefficiency from low-field areas on pixel boundaries/corners

High Voltage-CMOS

Benefit from industry standard high-voltage CMOS process.

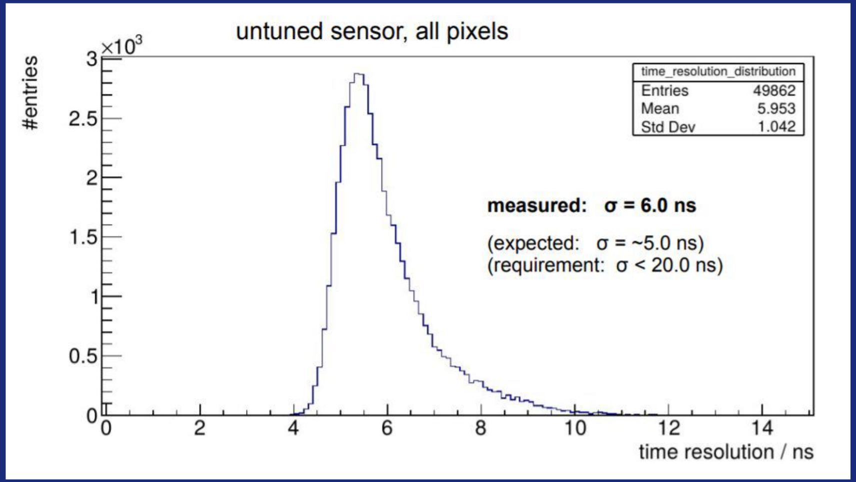
All electronics embedded in deep n-well, which acts as the collecting diode.

- Sensors can be full depleted (from the n-well) with bias voltages up to O(100 V) → fast charge collection
- Mostly vertical collecting field → high fill factor
- Large collection diode → higher noise and power

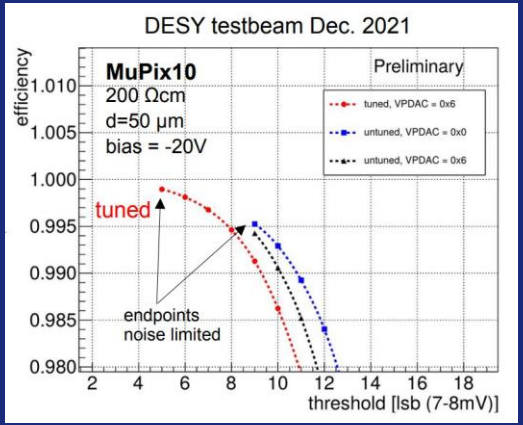

Ivan Peric NIM A 582 (2007) 876

MuPix11 – 150nm TSI

- 80 x 80 μm^2, thinned to 50 or 70 μm
- >99.9% efficient
- ~ 5 ns timing resolution



ATLASPIX (150 nm AMS) prototype was operated in test beam up to 1x10^{15} n$_{eq}$/cm^2



LHCbPIX - New chip under development for LHCb inner tracker upgrade

HV-MAPS back-biasing

Best radiation tolerance in planar silicon is achieved in n-in-p devices with V_{bias} approaching 1,000 V.
In MAPS devices HV is typically applied from the top-side.

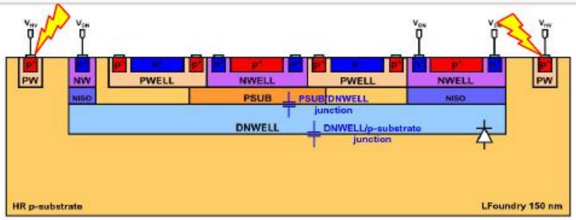
Shown in device simulation that much higher breakdown (~1000V) can be achieved in devices biased via (post processing) p^+ implant layer on the back of the sensor.

UKRI-MPW0 prototype:

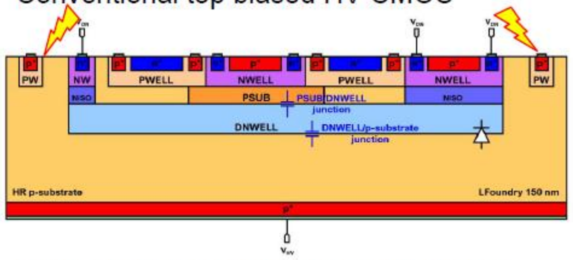
- Measured breakdown voltage above 600V
- Edge TCT measurements show
    - Full depletion at ~300V before irradiation (280 µm)
    - Over 50 µm depletion after $1x10^{16}$ n_{eq}/cm^2

Further prototypes submitted with improvements to sensor guard-rings and removal of topside bias contacts

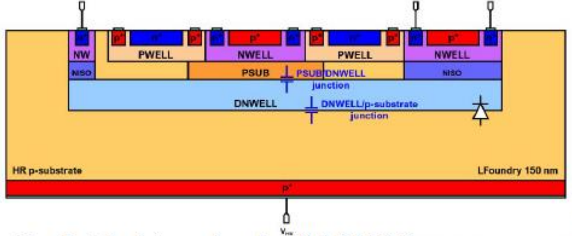
Similar R&D ongoing on Monopix-LF



Conventional top biased HV-CMOS

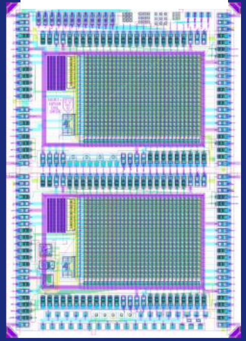


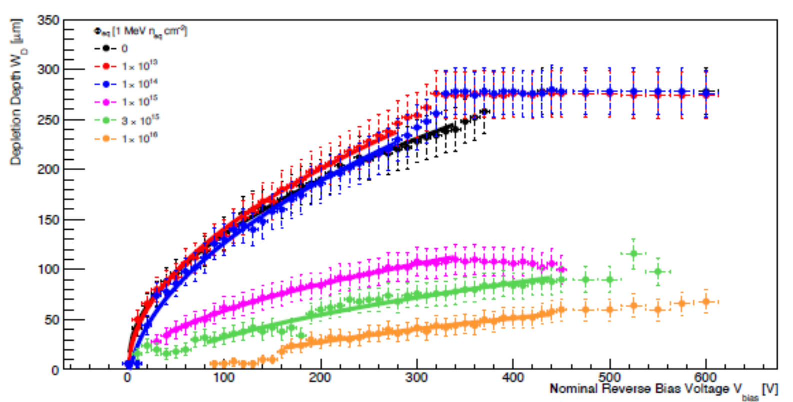
Backside biased HV-CMOS with floating topside p-wells



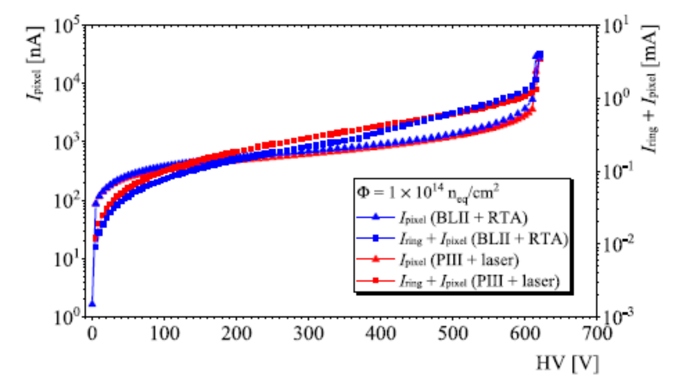
Backside biased only HV-CMOS
No topside biasing p-wells

UKRI-MPW0





Ben Wade IWoRiD 22



Ultra-Fast Silicon Detectors (UFSDs)

Motivation for fast timing

The 4D – tracking concept

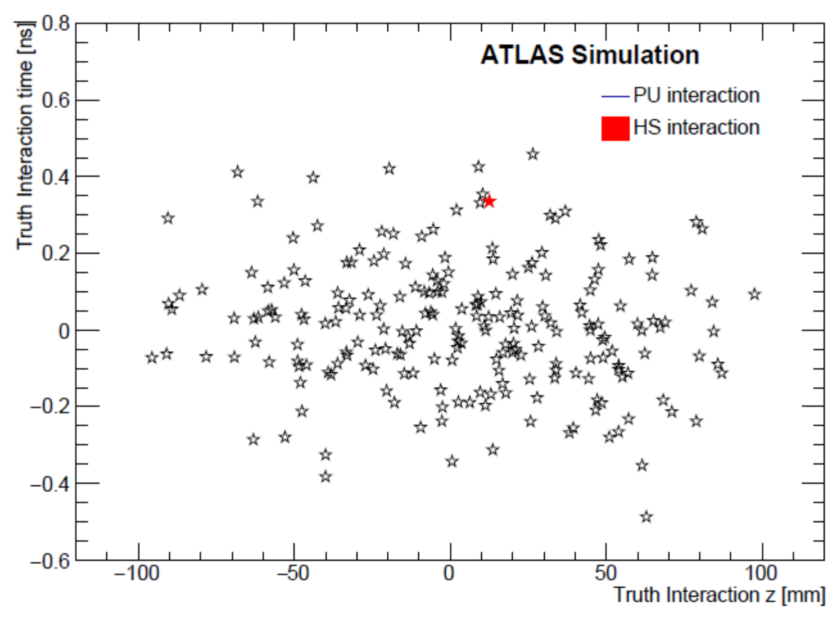
4D Tracking → based on hits with both spatial and timing information

- reduces the complexity of pattern recognition
- correctly associate tracks with vertices in pile-up events

Particle ID → time-of-flight measurements for particle ID

What is required?

1. excellent timing measurements (<50 ps),
2. unambiguously matched to tracks → *need adequate granularity*



Already possible using mixed technologies: e.g. pixel sensors combined with dedicated timing layers (scintillating fibres, LGADs, ..).

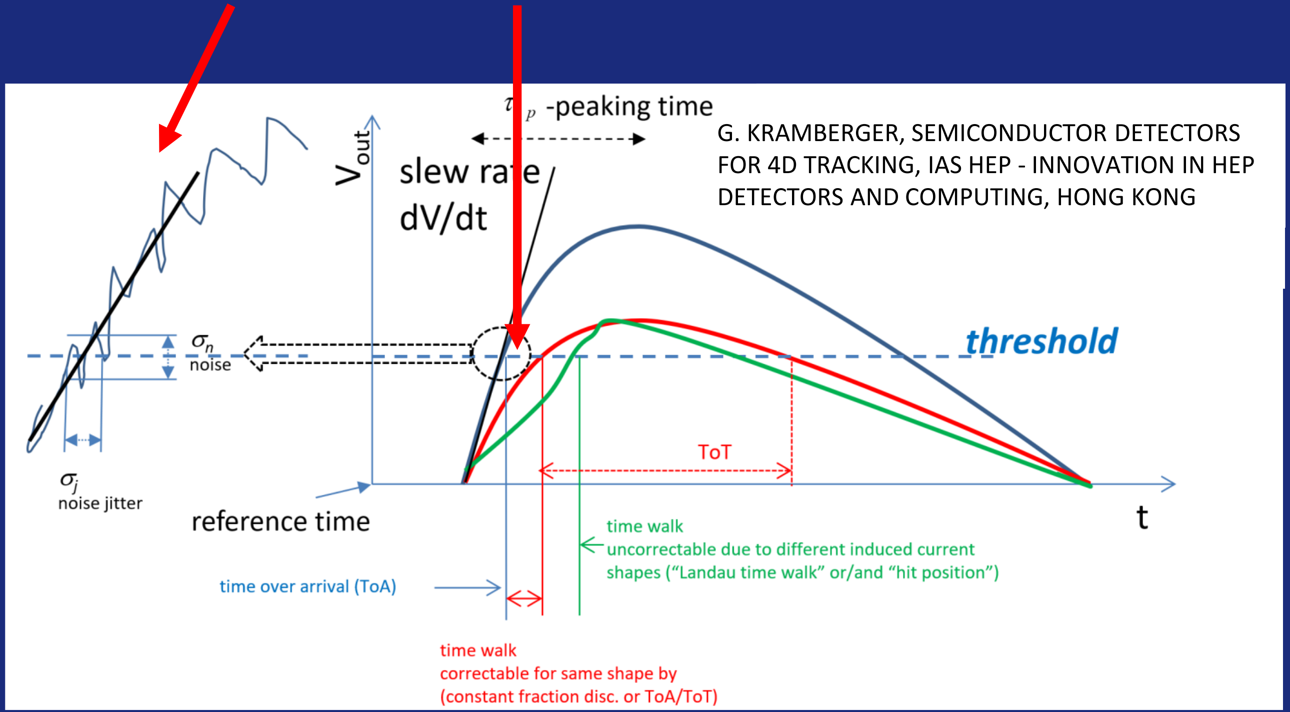
For high occupancy experiments (HL-LHC, FCC-hh, ..) we require high timing resolution pixelated devices, that also meet challenging radiation constraints.

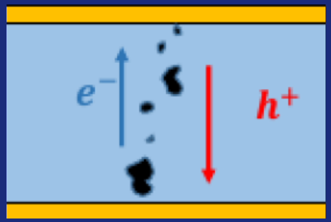
Ultimately full 4D tracking implies accurate timing and position information with every hit.

Time resolution

Many factors contribute to the timing resolution

$$\sigma_{Total}^2 = \sigma_{Jitter}^2 + \sigma_{Time\ Walk}^2 + \sigma_{TDC}^2 + \sigma_{Landau}^2 + \sigma_{Field}^2$$


G. KRAMBERGER, SEMICONDUCTOR DETECTORS FOR 4D TRACKING, IAS HEP - INNOVATION IN HEP DETECTORS AND COMPUTING, HONG KONG



How do we minimise these?

σ_{Jitter} (due to noise)

- → fast rise time
- → high S/N ratio (avoid thin devices!)

$\sigma_{Time\ Walk}$ (variation with amplitude)

- → can be corrected if amplitude is measured (ToT)

σ_{TDC} (resolution digitisation step)

- → large dynamic range TDC

σ_{Landau} (variation in ionisation charge with depth)

- → need short collection distance (thin devices)

σ_{Field} (local variations of the collecting field)

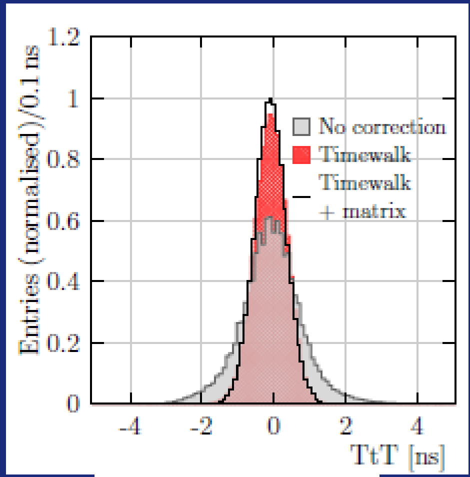
- → uniform E-field

Timing performance hybrid planar pixel sensors

Most devices are designed to meet the requirements of the LHC 40 MHz clock cycle.

For this ~10 ns is sufficient.

Is much faster possible?



arXiv : 2210.01442

Timepix4 bump-bonded on 100 µm pixel sensor (55 x 55 µm^2, 8ke/MIP)

- Full size, fully efficient, hybrid pixel device with fully functional ASIC

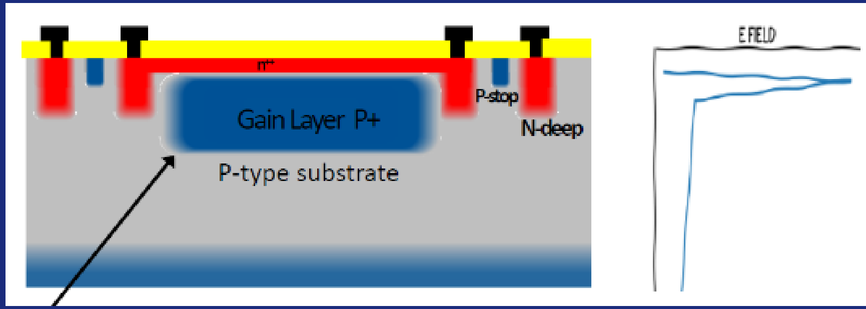
After time-walk corrections a time resolution of 440 ps was achieved

Achievable time resolution in planar silicon devices is limited because of the tension between reducing Landau and Jitter uncertainties

One solution is thin devices with gain!!

→ charge amplification inside the device can be achieved with local field strengths ~ 20 V/µm

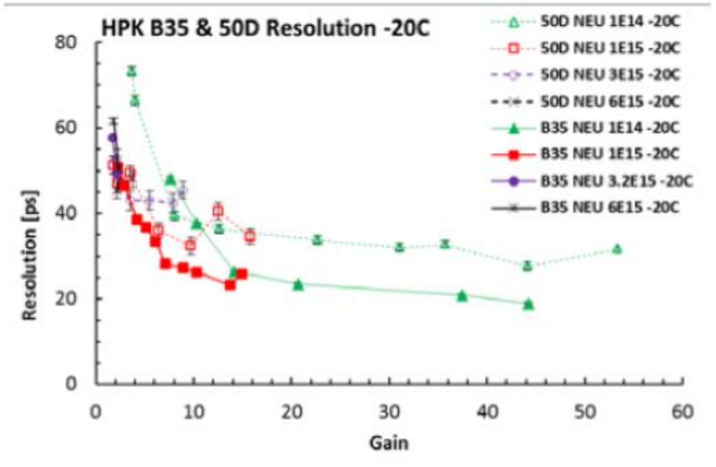
Low Gain Avalanche Diodes



Gain in planar devices can be achieved if the doping profile is modified to achieve a much higher electric field (E>20 V/μm).

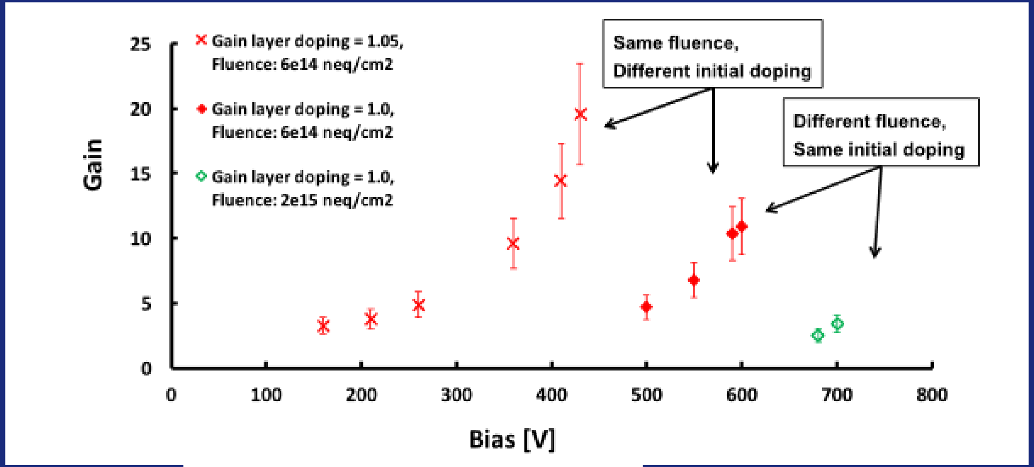
LGAD:

- p-in-n sensor, modified with p+ multiplication layer to create a high field region
- Operated at again of O(10-20) → timing resolution 20 - 30 ps
- Limited benefit higher gain once landau fluctuations dominate
- High E-field strength at the edges and corners of pixels necessitates pixel isolation with trenches. This limits minimal pixel sizes to ~ 1 x 1 mm^2).



Radiation tolerance:

- At high doses the gain is lost because of effective doping concentration changes in the gain layer. Can be compensated increasing the bias voltage.



Rep Prog Phys 81 026101, 2018.

ATLAS High Granularity Timing Detector

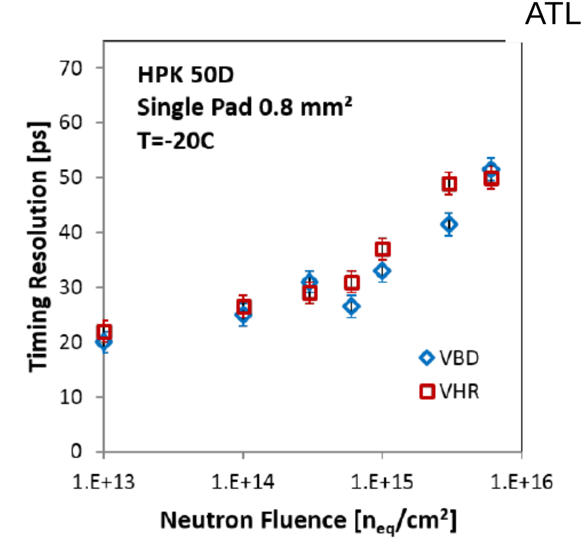
Pixelated LGAD detector at forward angles ($2.4 < \eta < 4.0$) to distinguish jets from hard scatter events from pile-up jets. This requires ~30ps timing resolution per track.

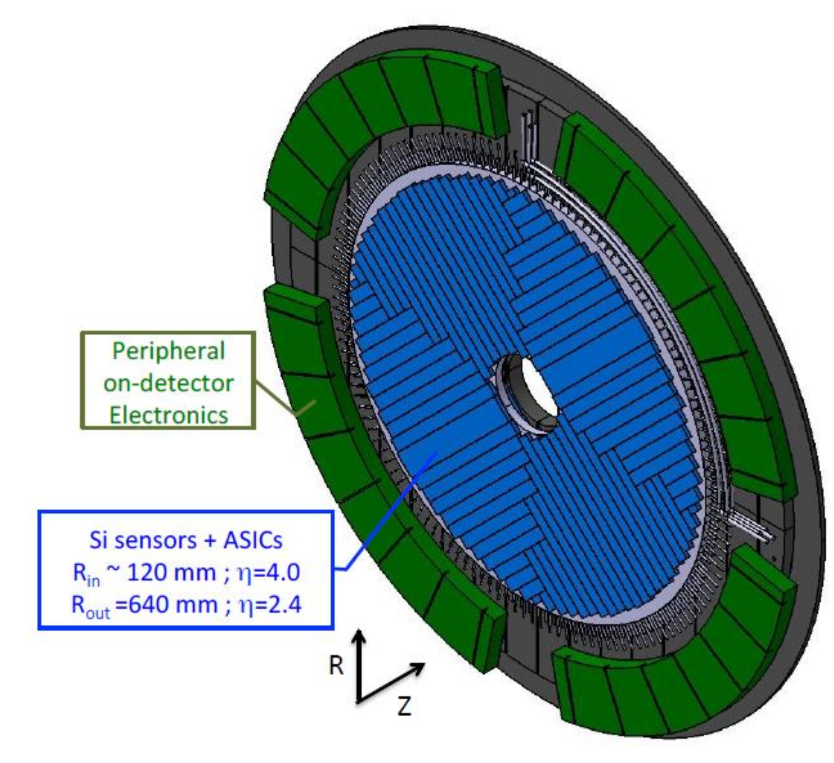
- LGAD sensors (1.3x1.3 mm^2)
- Bump bonded to custom ASIC
- operated at a gain of ~20

Performance

- Initial timing resolution 30 ps
- Expected to deteriorate to ~ 50 ps after full expected dose ($9\text{x}10^{15}$ n_{eq}/cm^2)

ATL-LARG-PROC-2018-003





Alternative approaches

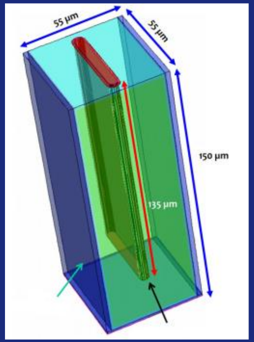
JINST 17 **P02019** *2022*

NIMA 981 (2020) 164491

Michela Garau, Trento 2023

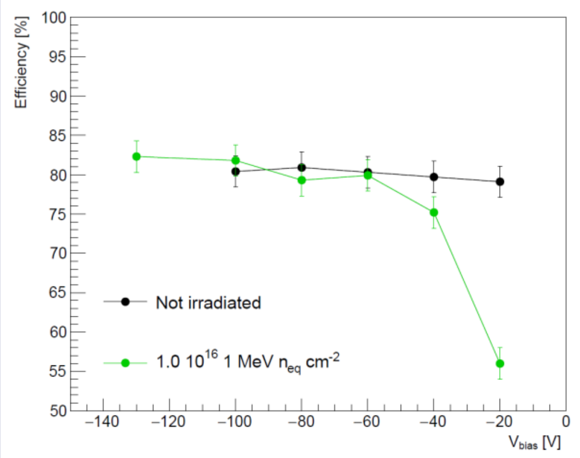
3D devices

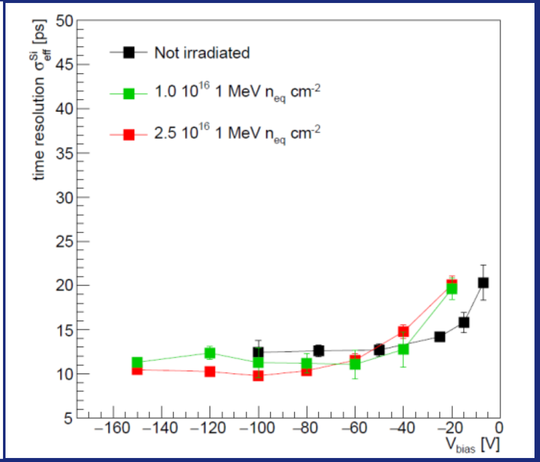
Limitation planar devices can be addressed decoupling the signal deposition depth (linked to S/N and thus σ_{Jitter}) from the charge collection path (linked to σ_{Landau}).



TIMESPOT: "parallel trench" 3D device, where the signal collection is perpendicular to charged article directions.

- Timing performance ~10 ps (analogue device only)
- efficiency substantially below 100%
- Performance retained up to 2.5x10^{16} n_{eq}/cm^2

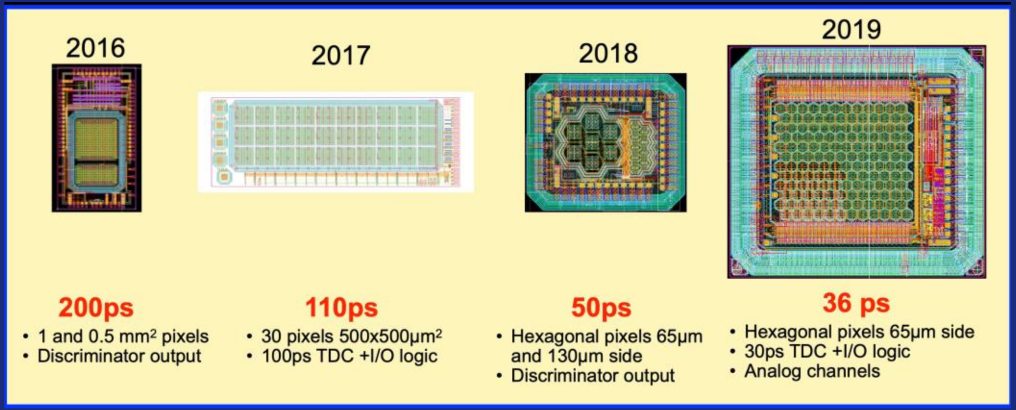




Monolithic SiGe BiCMOS

Development towards monolithic devices, benefitting from high charge mobility in SIGe devices. *(Technology used in high frequency electronics)*

Several prototype devices: SiGe without gain layer



MONOLITH programme

Towards SiGe BiCMOS with added gain layer

Target ~ 10 ps

Sensor R&D focus areas
Improved position resolution

Position resolution: the challenge

To first order hit position resolution in pixel detectors scales directly with the **pixel pitch.**
→ *smallest pixels sizes achieved to date are ~50x50 um^2 (hybrid) and ~18x18 um^2 (CMOS)*

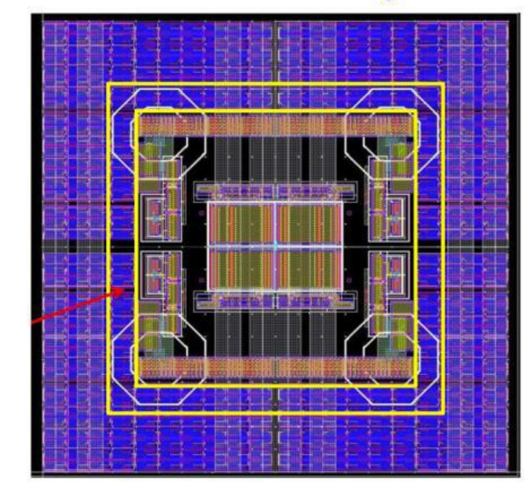
Position resolution is improved in case with **charge sharing**, using charge weighted position reconstruction.
→ *this requires devices that measure signal amplitude.*
Best performance in CMOS devices with charge collection by diffusion (e.g. ~3 µm in the MIMOSA chip)

Challenge:
Optimisation for high rates and radiation typically leads to devices with thin collection layer and high field → limited charge sharing

Can we go to much smaller pixels?

Separating analogue and digital electronics in very small pixels is challenging
There is only limited scope for reducing transistor size of analogue electronics, as this introduces noise and performance variations.

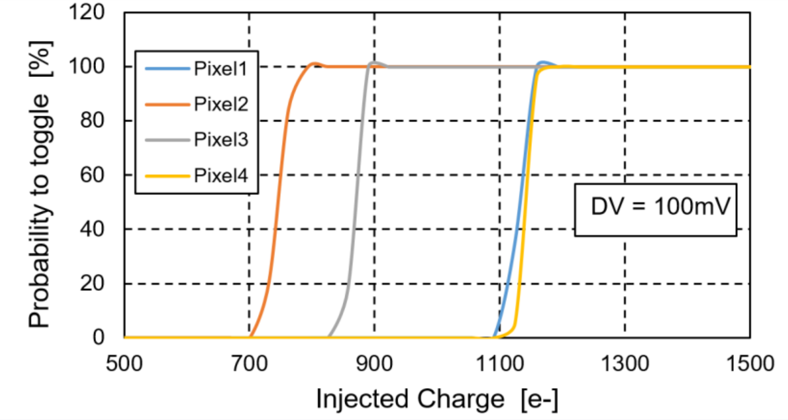
RD53: 4 readout pixels (50x50 µm^2) with shared analogue island



Novel concept: digital sensors for sub-micron pixels

Observation:

- state-of-the-art memory devices have “cell”-sizes far below 1 um^2 and …
- charged particles can induce bit flips in such devices (SEU: single event upsets).



JINST 17 (2022) 04 G. Casse et al

Fully digital pixel detector

- Demonstrator device implemented in 65nm UMC (2.5x2.5 um^2 pixels)
- re-engineered (SRAM) bit storage circuit for high sensitivity to radiation induced bit-flips

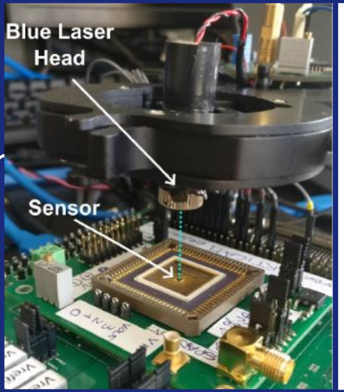
Difficult optimisation

- threshold charge (C_T) for inducing a bit flip depends on the detailed process parameters
- optimisation for very low C_T also induces leakage current that leads to false bit flips dark rate

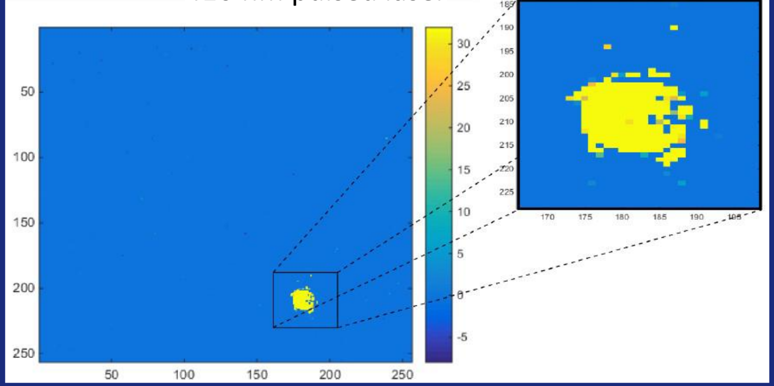
Results obtained at settings with negligible dark rate per second

- Detection threshold @ 1000 → *efficient for α-particles*
- *Laser spot measurement shows potential for micron level resolution*

Expectation that CT drops in smaller technology nodes



410 nm pulsed laser



Challenges of pixel sensor integration
Minimizing material

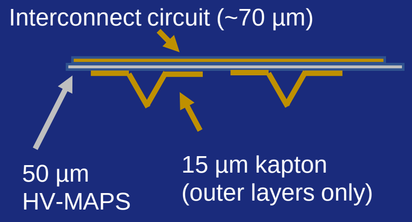
MAPS sensors thinned to 50 µm or less enables to build very low mass pixel arrays µm

Ultra low material pixel tracking
Mu3e pixel tracker

Mu3e has a unique requirement of ultra low material paired with fast timing

HV-MAPS sensors provide high efficiency and few ns timing resolution

Sensors can be thinned to 50 µm.



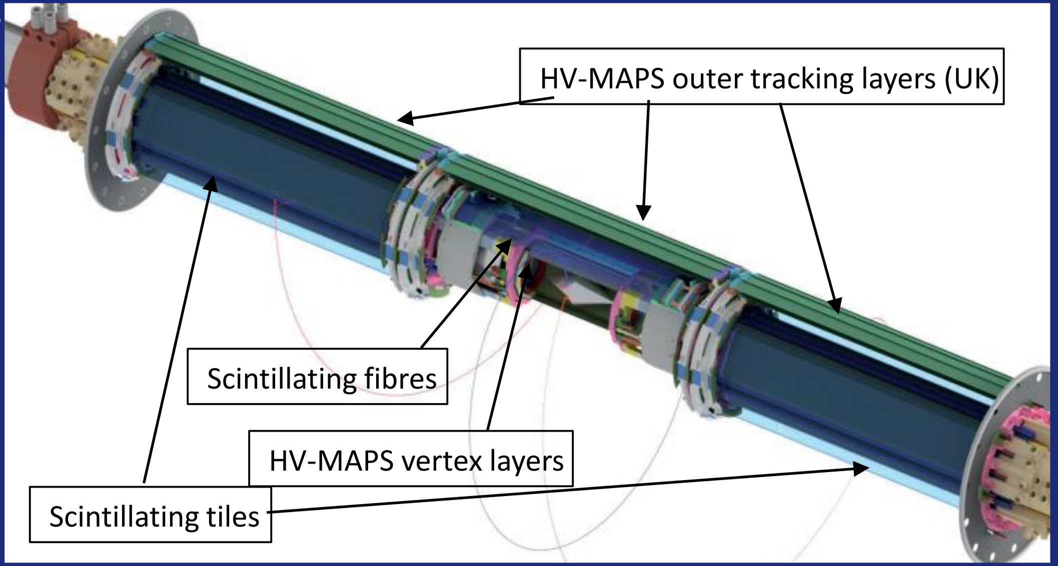
Mu3e pixel ladder consists of

- Between 6 and 18 50(70) µm MuPix sensors
- Glued and SpTAB bonded to a thin aluminium-kapton service flex.

Material per layer: ~0.11%X_0 per layer

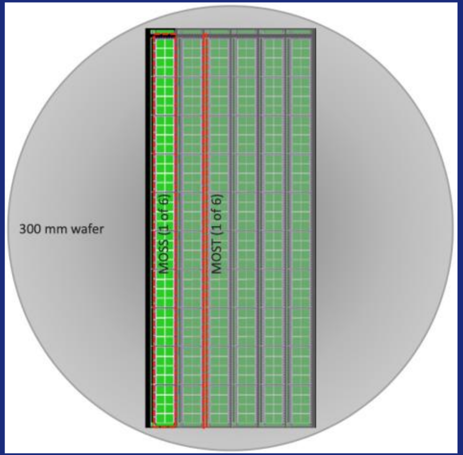
Full pixel array is cooled with high flow gaseous Helium

Extremely fragile detectors → very challenging construction



F.Carnesecchi, VERTEX 2022, ALICE ITS3

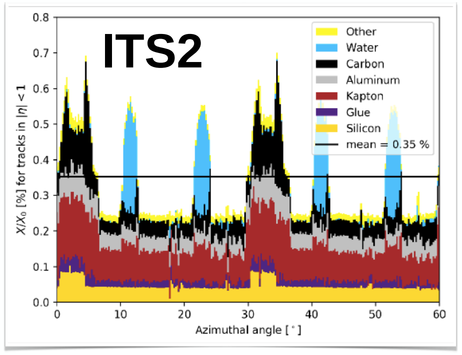
ALICE ITS3 barrel layer replacement

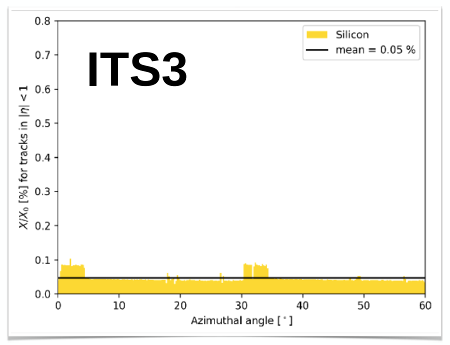


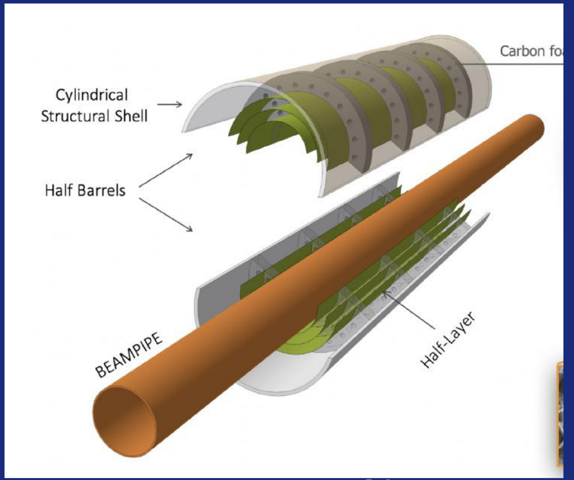
ALICE collaboration has ambitious aim to achieve a factor 7 improvement in material budget for its innermost pixel layers.

- In-vacuum vertex detector based on stitched wafer scale (280x94 mm^2) MAPS devices (stitching demonstrated in imaging devices) → in 65nm CIS TowerJazz,
- thinned to 20-40 µm and bent to half cylinder shapes.
- Mostly self-supporting, except for open carbon foam spacers
- Low power (20 mW/cm^2) to allow air cooling


Mechanical demonstrator
40-50 µm silicon







Total material budget ~0.02-0.04% X_0 per layer surrounding a 500 µm Be beampipe(0.14%

This brings a factor 2 improvement the impact parameter resolution

Summary

I discussed some of the challenges for pixel detector for future experiments and the R&D addressing these.

<u>High radiation</u>:
- Radiation tolerance beyond 10^{16} remains very challenging and still fully reliant on hybrid pixels
- Promising work on radiation hard monolithic sensors

<u>Timing</u>

- Very nice results from prototype devices (~10 ps looks achievable)
- Need this in fully functional devices, ideally monolithic with small pixels.

<u>Position</u>

- To make a big step, may need a fundamentally new approach (digital pixels?)

<u>Material</u>

- Active development work to go well below 0.1% X_0